

Project name: Libre-	Project number: 2021-	Most recent payment:
SOC Cavatools: Power	08-071	2024-08-30
ISA Simulator		

## **RfP Details**

Date	2024-08-30 at 14:09		
submit-			
ted:			
Payment:	no	Deliverables review:	Payment ap-
		pending	proval: pending
<b>Recipient</b> :	Luke Leighton		
984 Supp	ort SVP64 in cavatools		€5500

## *Subtask*wrapup

	Total amount requested for this task:€5500Total requested amount in this RfP:€5500
Results:	Top level page detailing main deliverables: <a href="https://libre-</a 
	<pre>soc.org/docs/pypowersim"&gt;https://libre- soc.org/docs/pypowersim/</pre>
	Tutorials: <a href="https://libre-&lt;/td&gt;&lt;/tr&gt;&lt;tr&gt;&lt;td&gt;&lt;/td&gt;&lt;td&gt;&lt;pre&gt;soc.org/docs/pypowersim_tut">https://libre- soc.org/docs/pypowersim_tut</a> /

Listed below: each task completed in the NLnet toplevel pypowersim project, with references to the relevant reports.

### Summary of PyPowerSim Documentation and Related
Work:

1. \*\*PyPowerSim Overview\*\*: PyPowerSim is a Pythonbased simulator for the OpenPOWER ISA, designed to aid in the development and testing of processor instructions. It supports instruction-level simulation for verifying correctness and performance.

[Documentation](<a href="https://libresoc.org/docs/pypowersim">https://libresoc.org/docs/pypowersim</a>/)

2. \*\*PyPowerSim Bug Fixes and Enhancements\*\*: Addressed issues related to instruction decoding and simulation accuracy, improving the simulator's reliability (Bug #758).

[Bug Report](<a href="https://bugs.libresoc.org/show\_bug.cgi?id=758">https://bugs.libresoc.org/show\_bug.cgi?id=758</a>)

3. \*\*PyPowerSim Tutorial\*\*: A comprehensive guide was created to help developers understand and utilize PyPowerSim effectively for simulating OpenPOWER instructions.

[Tutorial](<a href="https://libre-

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soc.org/docs/pypowersim_tut">https://libre-
soc.org/docs/pypowersim_tut</a>/)
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4. \*\*Development Logs\*\*: Logged detailed discussions and troubleshooting steps taken to resolve issues during the development of PyPowerSim, focusing on specific instruction implementations.

[IRC Log](<a href="https://libresoc.org/irclog/%23libre-soc.2023-09-10.log.html#t2023-09-10T18:44:49">https://libresoc.org/irclog/%23libre-soc.2023-09-10.log.html#t2023-09-10T18:44:49</a>)

5. \*\*PyPowerSim Source Code\*\*: The source code for PyPowerSim, including instruction decoders and other components, was maintained and updated to support ongoing development.

[Source Code](<a href="https://git.libre-soc.org/?
p=openpower-</pre>

isa.git;a=blob;f=src/openpower/decoder/isa/pypowersim
.py">https://git.libre-soc.org/?p=openpower-

isa.git;a=blob;f=src/openpower/decoder/isa/pypowersim
.py</a>)

6. \*\*HDL Workflow Scripts\*\*: Scripts were developed to streamline the HDL workflow, ensuring smoother integration between PyPowerSim and hardware development processes.

[HDL Workflow](<a href="https://libresoc.org/HDL\_workflow/devscripts">https://libresoc.org/HDL\_workflow/devscripts</a>/)

These accomplishments have significantly advanced the development and usability of PyPowerSim, making it a crucial tool in the OpenPOWER development ecosystem.

Remarks:

## Request status

Deliverables approval:	pending
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Transaction approval: pending

Payment no

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Make a new request

In case of questions or errors, send a mail.